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1 [The architecture of the Eden system](#)

Edward D. Lazowska, Henry M. Levy, Guy T. Almes, Michael J. Fischer, Robert J. Fowler, Stephen C. Vestal

December 1981 **Proceedings of the eighth ACM symposium on Operating systems principles**

Full text available:  [pdf\(827.67 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)



The University of Washington's Eden project is a five-year research effort to design, build and use an "integrated distributed" computing environment. The underlying philosophy of Eden involves a fresh approach to the tension between these two adjectives. In briefest form, Eden attempts to support both good personal computing and good multi-user integration by combining a node machine / local network hardware base with a software environment that encourages a high degree of shar ...

2 [Performance evaluation of software architecture: Using an architecture description language for quantitative analysis of real-time systems](#)

Robert Allen, Steve Vestal, Dennis Cornhill, Bruce Lewis

July 2002 **Proceedings of the third international workshop on Software and performance**

Full text available:  [pdf\(156.25 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#)



An architecture description language (ADL) specifies the structure of an overall system as an assembly of interacting components. ADLs can serve as input to a variety of development tools. We outline the Avionics Architecture Description Language, an emerging SAE standard for describing the architectures of hard real-time, safety-critical embedded computer systems. We describe a suite of tools that perform a set of verification, modeling and analysis, and implementation activities given an AADL ...

Keywords: embedded, fault-tolerant, real-time, software architecture

3 [Linear benchmarks](#)

Steve Vestal

October 1990 **ACM SIGAda Ada Letters**, Volume X Issue 8

Full text available:  [pdf\(690.95 KB\)](#) Additional Information: [full citation](#), [abstract](#), [citations](#), [index terms](#)



This paper presents a language feature benchmarking technique that is based on the use of multiple sampling loops and linear regression. Multiple performance estimates for multiple parameters can be obtained simultaneously. A heuristic is presented to automatically adjust the number of iterations for the sampling loops. It is also possible to compute values that give some insight into the accuracy of the estimates. This paper gives an overview of how such benchmarks may be coded and discusses so ...

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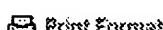
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VLSI Design, 2000. Thirteenth International Conference on , 3-7 Jan. 2000
Pages:530 - 537

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17 ASOC: a scalable, single-chip communications architecture

Jian Liang; Swaminathan, S.; Tessier, R.;
Parallel Architectures and Compilation Techniques, 2000. Proceedings.
International Conference on , 15-19 Oct. 2000
Pages:37 - 46

[\[Abstract\]](#) [\[PDF Full-Text \(1116 KB\)\]](#) **IEEE CNF**

18 High level modeling for parallel executions of nested loop algorithms

Deprettere, E.F.; Rijpkema, E.; Lieverse, P.; Kienhuis, B.;
Application-Specific Systems, Architectures, and Processors, 2000. Proceedings.
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Pages:79 - 91

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19 An energy balance simulation tool for TOMS-EP

Mackowski, M.J.; Martin, D.K.;
Energy Conversion Engineering Conference, 1996. IECEC 96. Proceedings of the
31st Intersociety , Volume: 1 , 11-16 Aug. 1996
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20 Defect oriented fault analysis for SRAM

Rei-Fu Huang; Yung-Fa Chou; Cheng-Wen Wu;
Test Symposium, 2003. ATS 2003. 12th Asian , 16-19 Nov. 2003
Pages:256 - 261

21 A modular simulation framework for architectural exploration of on-chip interconnection networks

Kogel, T.; Doerper, M.; Wieferink, A.; Leupers, R.; Ascheid, G.; Meyr, H.; Goossens, S.;

Hardware/Software Codesign and System Synthesis, 2003. First IEEE/ACM/IFIP International Conference on , 1-3 Oct. 2003

Pages:7 - 12

22 Design and FPGA implementation of a video scalar with on-chip reduced memory utilization

Ramachandran, S.; Srinivasan, S.;

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Pages:206 - 213

23 Current status and challenges of SoC verification for embedded systems market

Wooseung Yang; Moo-Kyeong Chung; Chong-Min Kyung;

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Pages:213 - 216

24 Specification, modeling and design tools for system-on-chip

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26 Digit-serial multiplier design using skew-tolerant domino circuits

Sungwook Kim; Sobelman, G.E.;

ASIC/SOC Conference, 2001. Proceedings. 14th Annual IEEE International , 12-15 Sept. 2001

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27 Direct-mapped asynchronous finite-state machines in CMOS technology

Sotiriou, C.R.;

ASIC/SOC Conference, 2001. Proceedings. 14th Annual IEEE International , 12-15 Sept. 2001
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28 Fast performance analysis of bus-based system-on-chip communication architectures

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29 Time-dependent aspects of the flow in the carotid bifurcation: continuous DPIV and computational results

Grad, Y.; Rosenfeld, M.; Yodfat, O.; Einav, S.;
[Engineering in Medicine and Biology, 1999. 21st Annual Conf. and the 1999 Annual Fall Meeting of the Biomedical Engineering Soc.] BMES/EMBS Conference, 1999. Proceedings of the First Joint , Volume: 1 , 13-16 Oct. 1999
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30 Proceedings Design, Automation and Test in Europe

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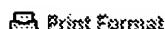
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1 Native ISS-SystemC integration for the co-simulation of multi-processor SoC

Fummi, F.; Martini, S.; Perbellini, G.; Poncino, M.;
Design, Automation and Test in Europe Conference and Exhibition, 2004.
Proceedings , Volume: 1 , 16-20 Feb. 2004
Pages:564 - 569 Vol.1

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2 Power estimation at architecture level for embedded systems

Mizuno, H.; Kobayashi, H.; Onoye, T.; Shirakawa, I.;
Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on , Volume: 2 , 26-29 May 2002
Pages:II-476 - II-479 vol.2

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3 SystemC cosimulation and emulation of multiprocessor SoC designs

Benini, L.; Bertozzi, D.; Bruni, D.; Drago, N.; Fummi, F.; Poncino, M.;
Computer , Volume: 36 , Issue: 4 , April 2003
Pages:53 - 59

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4 SimpleScalar: an infrastructure for computer system modeling

Austin, T.; Larson, E.; Ernst, D.;
Computer , Volume: 35 , Issue: 2 , Feb. 2002
Pages:59 - 67

[\[Abstract\]](#) [\[PDF Full-Text \(389 KB\)\]](#) **IEEE JNL**

5 A SystemC-based verification methodology for complex wireless software IP

Post, G.; Venkataraghavan, P.K.; Ray, T.; Seetharaman, D.R.;
Design, Automation and Test in Europe Conference and Exhibition, 2004.
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Alok Jain, Randal E. Bryant

June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**

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42 [HDR and tone mapping: Interactive time-dependent tone mapping using programmable graphics hardware](#)

Nolan Goodnight, Rui Wang, Cliff Woolley, Greg Humphreys

June 2003 **Proceedings of the 14th Eurographics workshop on Rendering**

Full text available: [pdf\(7.56 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)



Modern graphics architectures have replaced stages of the graphics pipeline with fully programmable modules. Therefore, it is now possible to perform fairly general computation on each vertex or fragment in a scene. In addition, the nature of the graphics pipeline makes substantial computational power available if the programs have a suitable structure. In this paper, we show that it is possible to cleanly map a state-of-the-art tone mapping algorithm to the pixel processor. This allows an inter ...

43 [Design and verification of the Rollback Chip using HOP: a case study of formal methods applied to hardware design](#)

Ganesh Gopalakrishnan, Richard Fujimoto

May 1993 **ACM Transactions on Computer Systems (TOCS)**, Volume 11 Issue 2

Full text available: [pdf\(2.52 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)



The use of formal methods in hardware design improves the quality of designs in many ways: it promotes better understanding of the design; it permits systematic design refinement through the discovery of invariants; and it allows design verification (informal or formal). In this paper we illustrate the use of formal methods in the design of a custom hardware system called the "Rollback Chip" (RBC), conducted using a simple hardware design description language called "HOP&r ...

44 [Caches and Memory Systems: A vision for embedded software](#)

Alberto Sangiovanni-Vincentelli, Grant Martin

November 2001 **Proceedings of the international conference on Compilers, architecture, and synthesis for embedded systems**

Full text available: [pdf\(169.62 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)



In this paper we describe a vision for the future evolution of Embedded SW (ESW) design methodologies as part of overall Embedded Systems (ES) development. Fundamentally, we believe that the way in which embedded SW is developed today must change radically. The